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EXAMINER	
THAI, TUAN V	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	09/212,291	PRUDVI ET AL.	
	Examiner	Art Unit	
	Tuan V. Thai	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 May 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7,11-16,25 and 26* is/are pending in the application.

4a) Of the above claim(s) *8-10,17-24 and 27-29* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7,11-16,25 and 26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Part III DETAILED ACTION

1. This office action is in response to Applicant's communication filed May 18, 2005 following the decision from the Board of Patent Appeals and Interferences wherein the rejection of claims 17-21, 23-24 and 27-29 under 35 U.S.C. § 102 as being anticipated by Scales is affirmed; the rejection of claims 1-7, 11-16, 25, and 26 under 35 U.S.C. § 103 as being unpatentable over Sachs and Scales is reversed. Claims 17-21, 23-24 and 27-29 are therefore being withdrawn from further consideration. Claims 8-10 and 22 have been canceled. Claims 1-7, 11-16 and 25-26 are therefore presented for examination.

2. Applicant's arguments with respect to claims 1-7, 11-16 and 25-26 have been considered but are deemed to be moot in view of the new grounds of rejection.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claim 1 is rejected under 35 U.S.C. 102(e) as being anticipated by DeKoning (USPN: 6,148,368).

As per claim 1, DeKoning discloses a processing agent as being equivalent to controller 202 for transferring data of a predetermined data length in an external transaction (e.g. see figure 2; column 6, lines 46-64), the controller comprising in internal cache memory 224 (e.g. see figure 2, column 6, lines 61-64) having plurality of cache entries/ segments [225, 226, 228 and 230] being equivalent to cache entries 510 of cache 500 (Applicant's figure 2, and specification's page 5, lines 6 et seq.), each entry/ segment sized to store multiple data line lengths of data; for example, DeKoning teaches these cache segments vary in size, and the various cache sized segments are non-uniform in size according to the specific needs of the application (e.g. see column 8, lines 43-47).

Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1-7, 11-16 and 25-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sachs et al. (USPN: 4,884,197); hereinafter Sachs, in view of DeKoning (USPN: 6,148,368).

As per claim 1, Sachs teaches the invention as claimed including a processing agent (e.g. see figures 8 and 9) to transfer data of predetermined data length in an external transaction, the agent comprising an cache memory 320 having a plurality of cache entries; for example, Sachs discloses that the cache memory 320 having three fields, a used bit field, and two identical read-write memory fields W and X wherein each field W and X contain multiple lines, and each line in the cache contains multiple entries

(fields) (e.g. see figure 10.B) and having tag field RA, line valid bit LV, line dirty bit LD and multiple data entries DT (e.g. see column 22, lines 14 et seq.). Sachs discloses the invention as claimed; however Sachs does not particularly teach that each entry sized to store multiple data line lengths of data. DeKoning, in his teaching of segmented cache memory for accelerating disk array write operation, disclose the missing element that is known to be required in Sachs in order to arrive at Applicant's current invention wherein DeKoning teaches dynamic cache memory 224 (e.g. see figure 2) having a plurality of cache segments/ entries [225, 226, 228 and 230] being equivalent to cache entries 510 of cache 500 (Applicant’s figure 2, and specification’s page 5, lines 6 et seq.), wherein these cache segments vary in size; DeKoning discloses the various cache sized segments are non-uniform in size according to the specific needs of the application, other words; the size of the cache segments are system dependent feature (e.g. see column 8, lines 43-47). DeKoning clearly discloses by utilizing the variable cache sized segments/ entries, it would provide an ease in cache scaling to adapt performance (e.g. see column 3, lines 64 bridging column 4, line 7); in addition, by using variable size cache

segments, it would reduce the number of cache write cycles to cache 224 since additional cache write would have required to fill the fixed cache segments/entries before data can be transferred to disk array 210. Accordingly, it would have been obvious to one having ordinary skill in the art at the time the current invention was made to implement the cache having multiple cache entries or segments, wherein each segment sized to store multiple data line lengths of data as taught by DeKoning for that of Sachs. In doing so, it would (a) allow the cache to be easily scaled to adapt performance, clearly to allow Sachs's system to serve broader range of applications, therefore increasing system adaptability, and (b) increasing throughput of write operation by reducing number of cache write cycles to cache, therefore being advantageous.

As per claim 2, Sachs clearly discloses that the cache entries include a tag portion for storing address information as being the real address field RA (e.g. see figure 10B, and column 22, lines 32 et seq.).

As per claim 3, the match detection logic for the tag portions and control logic provided in communication with the match detection logic is taught by Sachs as the comparators 332 and 334, and the multiplexer 341 (e.g. see

figure 9, column 21, lines 4 et seq.; for example, Sachs discloses the match/no match signals output from comparators 332 and 334 indicate a cache hit when the requested real address was presented in the cache and the data was valid, or a cache miss when the requested data is not present in the cache (e.g. see column 21, lines 20 et seq.).

As per claim 4, Sachs clearly teaches each cache line further have a cache coherency state field such that: a cache line valid bit LV, a line dirty bit DT (e.g. see figure 10B, column 22, lines 28 et seq.).

As per claim 5, Sachs discloses his processing agent further comprising a transaction queue as being equivalent to the TLB 350 having a plurality of queue entries (lines) (e.g. see column 22, line 54 et seq.), wherein the queue entries including a primary entry for storing address information and status information of a first external transaction, and a secondary entry for storing status information of a second external transaction is explicitly taught by Sachs as each line having virtual address field VA for storing address information and a reference bit R field or a dirty bit D field for storing status information of an external transaction being read/write transactions

(note also an user valid bit UV field, a supervisor valid bit field, a protection level word PL field and a system tag ST field; e.g. see column 22, lines 59 et seq.; column 24, lines 27 et seq.).

As per claim 6, Sachs further discloses the status information of the first external transaction includes a field (e.g. the reference bit R or the dirty bit D) indicating that the line has been referenced by a read or write transaction (multiple transaction sequence), or having been modified by a write transactions (e.g. see column 22, lines 59 et seq.; column 24, lines 27 et seq.).

As per claim 7, Sachs discloses the invention as claimed; however Sachs does not particularly teach that the total number of primary and secondary entries equals to the number of data line lengths provided in the cache entries. First of all, it should be noted that the total number of lines in both cache and TLB being disclosed in Sachs's system is a system dependent feature, it can be varied dependent on what system they are implemented within. Secondly, Sachs clearly discloses the W and X memories in BOTH cache memory 320 and TLB 350 each contain multiple lines, and as an example for illustration in the current invention, Sachs selects the number of cache lines being

equal to 128 lines (column 22, line 22); and the number of lines in the TLB is 64 lines (e.g. see column 22, line 54). Accordingly, it would have been obvious to one having ordinary skill in the art at the time the current invention was made to implement both cache and TLB to have the same number of lines since the numbers of lines in both cache and TLB are changeable as indicated by Sachs. In addition, doing so, it would allow the TLB to buffer more data for reference which results to increasing data hit rate in both TLB and cache, therefore being advantageous.

As per claim 11; Sachs disclose a processing agent (e.g. see figures 8 and 9) comprising an cache memory 320 having a plurality of cache entries; for example, Sachs discloses that the cache memory 320 having three fields, a used bit field, and two identical read-write memory fields W and X wherein each field W and X contain multiple lines, and each line in the cache contains multiple entries (fields) (e.g. see figure 10.B) and having tag field RA, line valid bit LV, line dirty bit LD and multiple data entries DT (e.g. see column 22, lines 14 et seq.). A transaction queue system as being equivalent to the TLB 350 having a plurality of queue entries (lines) to post external transactions, each external transaction related to

a single data line (e.g. see column 22, line 54 et seq.), wherein the internal cache and the transaction queue system each receive data requests on a common input (e.g. see figure 8 show common input line being connected to both TLB 270 and cache 220). Sachs discloses the invention as claimed; however Sachs does not particularly teach that each entry sized to store multiple data line lengths of data. DeKoning, in his teaching of segmented cache memory for accelerating disk array write operation, disclose the missing element that known to be required in Sachs in order to arrive at Applicant's current invention wherein DeKoning teaches dynamic cache memory 224 (e.g. see figure 2) having a plurality of cache segments/entries [225, 226, 228 and 230] being equivalent to cache entries 510 of cache 500 (Applicant’s figure 2, and specification’s page 5, lines 6 et seq.), wherein these cache segments vary in size; DeKoning discloses the various cache sized segments are non-uniform in size according to the specific needs of the application, other words; the size of the cache segments are system dependent feature (e.g. see column 8, lines 43-47). DeKoning clearly discloses by utilizing the variable cache sized segments/entries, it would provide an ease in cache scaling to adapt performance (e.g. see column 3,

lines 64 bridging column 4, line 7); in addition, by using variable size cache segments, it would reducing number of cache write cycles to cache 224 since additional cache write would have required to fill the fixed cache segments/entries before data can be transferred to disk array 210. Accordingly, it would have been obvious to one having ordinary skill in the art at the time the current invention was made to implement the cache having multiple cache entries or segments, wherein each segment sized to store multiple data line lengths of data as taught by DeKoning for that of Sachs. In doing so, it would (a) allow the cache to be easily scaled to adapt performance, clearly to allow Sachs's system to serve broader range of applications, therefore increasing system adaptability, and (b) increasing throughput of write operation by reducing number of cache write cycles to cache, therefore being advantageous.

As per claim 12, Sachs discloses the internal cache and the transaction queue system communicate by signal lines (e.g. see Sachs's figure 8).

As per claim 13, Sachs further discloses the signals line include a cache hit signal line and a tag hit signal

line (e.g. see figure 9, column 19, lines 58 et seq.; column 20, lines 4 et seq.).

As per claim 14, Sachs teaches the invention as claimed including a processing agent comprising a transaction queue as being equivalent to the TLB 350 having a plurality of queue entries (lines) (e.g. see column 22, line 54 et seq.), wherein the queue entries further comprising a primary sub entry including an address information and status information provided for a first external transaction, and a secondary subentry provided including a status portion provided for a second external transaction is explicitly taught by Sachs as each line having virtual address field VA for storing address information and a reference bit R field or a dirty bit D field for storing status information of first external transaction being read/write transactions (with respect to status for the second external transaction, note also an user valid bit UV field, a superior valid bit field, a protection level word PL field and a system tag ST field; e.g. see column 22, lines 59 et seq.; column 24, lines 27 et seq.).

As per claim 15, the further limitation of wherein the status portion of the primary entry includes a field

representing whether the first transaction is part of a multiple transaction queue is equivalently taught by Sachs as the reference bit R or the dirty bit D field of each line indicating that the line has been referenced by a read or write transaction (multiple transaction sequence), or having been modified by a write transactions (e.g. see column 22, lines 59 et seq.; column 24, lines 27 et seq.).

As per claim 16, Sachs discloses the TLB control logic unit 820 as being equivalent to the control logic being claimed, coupling to the TLB 350 for cycle through the queue entries and post transaction therefrom (e.g. see Sachs's figure 23).

As per claims 25 and 26, wherein data line corresponds to the maximum amount of data that can be transferred in a single bus transaction is taught by Sachs to the extent that it is being claimed; for example, when detailing data cache bus, Sachs discloses on store operations, the CPU puts an address following by data on the address/data bus for one (single) clock/bus cycle (e.g. see column 6, lines 27 et seq.).

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tuan V. Thai whose telephone number is (703)-305-3842. The examiner can normally be reached on from 6:30 A.M. to 4:00 P.M..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mathew M. Kim can be reached on (703)-305-3821. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TVT/April 14, 2008

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